

Fig. 18

Linear CCD specifications for storage-phosphor image plate reading

CCD architecture	Linescan (photosites & single register)
Photosite dimension	220 μm high x 44 μm wide (44 μm pitch)
Photosite design	5 photogates/pixel (44 μm high x 4 μm wide)
Shift register cell dimension	60 μm x 44 μm on a 44 μm pitch
Shift register design	2poly/2 ϕ or 4 ϕ switchable (with center split)
Shift register operation	Uni or bidirectional 2 ϕ or 4 ϕ (MPP mode)
Pixel count	2048 pixels
Die size	90.1 mm x 2.25 mm
Total dark current	< 20 pA/cm ² MPP mode at 25°C
Shift register dark current (MPP mode)	25e ⁻ /cell for 2ms integration at 40°C
Photogate charge transfer inefficiency (lag)	< 50e ⁻ at 1000 e ⁻ signal level
Well Capacity	10 ⁶ e ⁻
Amplifier readout noise	5 e ⁻ at 250 kHz (single-stage amplifier)
Output configuration	1 or 2 outputs in split mode (opposite ends)
Effective Quantum Efficiency (uncoated)	> 50% at 400nm (63% QE x 80% FF)
Effective Quantum Efficiency (AR coated)	> 75% at 400nm (94% QE x 80% FF)
Open photogate fill factor (no poly coverage)	> 80%
Maximum readout speed	500 kHz
Binning	4x
Charge Transfer Efficiency	0.99999
Buttability	3 side buttable (< 22 μm dead space)

